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10/069,806	05/13/2002	Christian Paulus	32226.18	7278

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/069,806	PAULUS ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,16 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,16 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is responsive to the amendment filed on 03-05-04. The amended figure 3 is not acceptable and the 112, second paragraph problem still exists.

Drawings

The drawings are objected to because the amended figure 3 is not seen to be correct. The newly submitted figure 3 is not acceptable for the following reasons:

a) The gate of transistors (22) and (32) are biased by **fixed power supplies**. Thus, it is not rational to connect the "input signal " (13) to these two power supplies.

b) **The newly added line** that connects node **(13)** to **node (11) is not electrically correct** because the output node (11) of circuit (50) **cannot be connected to the input signal** (13). The signal at node (11) or the output signal of circuit (50) is seen to be a control signal for two sub-driver circuits (20) and (30).

c) Figures 1, 2 and the amended figure 3 shows that the evaluation circuits (50, 60) receive both the feedback signal (from node 12 in figure 3) and the **input signal** (13). These connections are not correct. As seen in the old figure 3, the input signals are only applied to transistors (23) and (33) of the sub-driver circuits. The connection between input signal (13) and the evaluation circuits (50, 60) in figures 1, 2 and amended figure 3 should be removed. The lines that connect input signal (13) to the two bias supplies in amended figure 3 should be removed also.

d) In figure 3, inverter (53, 54) has the input coupled to its output. This connection line should be removed. The connection between inverter (53, 54) and (56, 57) is not well defined.

e) The **blank boxes** in figures 1 and 2 must have **functional labels.**

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed

from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: the disclosure "the at least one input node for the input signal may be connected to the at least one evaluation circuit" in page 6, first paragraph is misleading because the old figure 3 of the present application shows that the **input signal** cannot be connected to the **output** of the evaluation circuit.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-14, 16 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitation "wherein a second terminal of the first transistor of the first polarity and a second terminal of the first transistor of the second polarity are coupled to each other and to the **input node of the evaluation circuit**" is indefinite because it is not clear how the **input** and the **output** of inverter (53, 54) can be coupled to the **same input node** (51). With this connection, the output and the input of inverter (53, 54) are shorted together. The recitation "wherein a second terminal of the second transistor of the first

polarity and the second terminal of the second transistor of the second polarity are **coupled to each other** and to the **input node** for the input signal" on lines 17-19 is indefinite because it is misdescriptive. The "old" figure 3 shows that the second terminal of the second transistor of the first polarity (57) and the second terminal of the second transistor of the second polarity (56) are coupled to each other and to **control terminals of transistors** (24) and (34) of the sub-drivers (20) and (30). As mentioned in the drawing objection, node (11) in figure 3 of the amended drawing **cannot be the input node** of the driver circuit because node (11) is the **output** of the evaluation circuit (50) and this output electrically **cannot be connected** to the **input signal** (13). The Applicant is respectfully requested to point out in the amended figure 3 of the present application what is the "real" input node of the driver circuit.

Regarding claim 3, the recitation "wherein the input node for the **input signal** is connected to the **evaluation circuit**" is indefinite for the same reason previously described.

Claims 2, 4-14, 16 and 17 are indefinite because of the technical deficiencies of claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6, 7-10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawabata (US Pat. 6,650,152) in view of Talbot (US Pat. 6,445,253) further in view of McPartland et al. (US Pat.6, 552,931) and Gaalema (US Pat. 5,523,864).

Regarding claims 1, 2 and 3, figure 3 of Kawabata shows driver circuit, having at least one input node (30) for an input signal and at least one output node (10) for an output signal, having one or more, preferably two, sub-drivers (37, 11) and (38,12), and having a feedback circuit (20, 36), which has one or more evaluation circuits (20, 36), the at least one evaluation circuit having a first inverter stage (20), coupled to the input node of the evaluation circuit,

and a second inverter stage, coupled with the first inverter stage, the first inverter stage inherently comprising at least a first transistor of a first polarity and a first transistor of a second polarity, the second polarity being different from the first polarity, wherein the control terminal of the first transistor of the first polarity and the control terminal of the first transistor of the second polarity are coupled to the input node of the evaluation circuit, wherein the second inverter stage comprises at least a second transistor of the first polarity and a second transistor of the second polarity, and wherein a second terminal of the second transistor of the first polarity and a second terminal of the second transistor of the second polarity are coupled to each other and to the sub-driver circuits. The circuit of Kawabata does not show feedback capacitor(s). However, it is old and well known in the art that a capacitor when installed on a signal line block dc component of the signal (see US Pat. 6,445,253). Therefore, it would have been obvious to those skilled in the art at the time the invention was made to implement feedback capacitor(s) between the output node and the evaluation circuit (2) for blocking the DC component that cause offset effect in the circuit. Note that the input signal (39) is coupled to the sub-driver circuits. The input node is connected to the sub-driver circuits.

Regarding claim 6, the evaluation circuit of Kawabata and the evaluation circuit of the present application are inverters thus, inherently they both have low input impedance.

Regarding claim 7, the sub-driver (37, 11) comprises one or more transistors.

Regarding claim 8, it is inherent that each sub-driver that is connected to the evaluation circuit comprises control transistor as input transistor.

Regarding claims 9 and 10, the combination of Kawabata and Talbot includes all the limitations of the present applications except for the limitation that the feedback capacitor is a linear capacitor, in claim 8; or a non-linear capacitor, in claim 9. However, the type of capacitors used as coupling capacitor (feedback capacitor) is deemed to be obvious to those having skill in the art as merely routine design expedient. For instance the linear capacitor is used to provide an output that varies linearly with respect to the voltage applied to the input of the capacitor (see US Pat. 6,552,931). A non-linear capacitor is used if the coupling capacitor needs to have a capacity that is almost independent of the applied voltage (See US Pat. 5,523,864).

Regarding claim 11, figure 1 of McPartland shows that the non-linear capacitor is formed from MOS transistor (PMOS).

Response to arguments

In the Remarks, page 10, the Applicant states that "It is note on the amended drawing that the **input node** also functions as the **connectetion between the pull up sub-driver** (20) and the **pull down driver** (30). Thus, the **valuation circuit** (50) is connected to the **input node** (11) and the sub-drivers (20, 30)". This statement is not seen to be correct. The "**old**" figure 3 of the present application shows a driver circuit comprising **two input nodes** (the gates of transistors 23 and 33); a feedback circuit (50); two sub-driver circuits (20, 30). Sub-driver circuits (20, 30) both receive feedback signal from the output (11) of the feedback circuit (50) that is applied to the gates of transistors (24 and 34). **Node (11) is the output of circuit (50), not the input of the driver circuit** as stated. In the amended figure 3, the Applicant modifies the drawing so that the "input signal" (13) is coupled to both bias supplies that bias the gates of transistors (22) and (32) and to the output (11) of circuit (50). Electrically this kind of connection is not acceptable because node (11) is the **output** of circuit (50) and the two bias power supplies cannot be controlled by the input signal (13). The Applicant is requested to clarify what is the **real** input of the driver circuit and to explain why the **input signal** (13) can be inputted to the **output** (11) of the "evaluation circuit" (50) and to two bias power supplies that bias the gates of transistors (22) and (32).

Allowable Subject Matter

Claims 4, 5, 12-14, 16 and 17 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
07-27-04

TUAN T. LAM
PRIMARY EXAMINER